Intellectual Property Office

BL O/749/21

11 October 2021

PATENTS ACT 1977

APPLICANT	Imagination Technologies Limited
ISSUE	Whether patent application GB1805684.6 complies with section 1(2)
HEARING OFFICER	B Micklewright

DECISION

Introduction

1 Patent application GB1805684.6, titled 'Evaluating a mathematical function in a computational environment', was filed in the name of Imagination Technologies Limited on 5 April 2018.The application makes no priority claim, and was published on 9 October 2019 as GB2572622 A.

2 While a combined search and examination was requested by the applicant, the initial action issued by the examiner was an abbreviated examination in which the examiner argued that the invention was excluded from patentability as it related to a computer program as such. Due to this objection, the examiner issued a search report under section 17(5)(b) of the Patents Act 1977 ('the Act') stating that a search would serve no useful purpose.

3 A number of rounds of amendments and further examination reports followed, with the examiner maintaining that the invention relates to a computer program as such and/or to a mathematical method as such. A hearing was suggested by the examiner in their report of 2 October 2020 and requested by the applicant in their response of 2 February 2021. The matter came before me at a video hearing on 21 July 2021, with the applicant being represented by Mr Stephen Turner of Slingsby Partners and by Mr Dan Cooney from Imagination Technologies.

4 I am grateful for Mr Turner and Mr Cooney for the extensive skeleton arguments which were provided to me prior to the hearing. I confirm that I have taken account of these in reaching my decision. I have also reviewed the correspondence on file.

The Invention

5 The application is directed towards an apparatus and method for evaluating a mathematical function in a computational environment. It is stated that within a computational environment it is often necessary to compute certain mathematical functions for given input values, such as floating point or fixed-point numbers.

6 There are a number of approaches which can be taken to evaluate such mathematical functions. One approach involves approximating the function with a polynomial and then evaluating the polynomial for the given input value. In order to attain a desired level of accuracy, it is common to divide the domain of a function into a number of intervals which are each calculated separately, with a greater number of intervals resulting in a higher level of accuracy. As it is necessary to store sets of values, for example one or more coefficients of a polynomial equation, for each interval, a higher level of accuracy requires a proportionally larger amount of storage.

7 Another approach is to implement an iterative operation such as performing a CORDIC algorithm. With such an approach, the accuracy of the operation is not dependent on stored values but rather on the number of iterations of the operations performed.

8 The invention seeks to address the issue of storage requirements by evaluating a mathematical function in a two-step process. Firstly, a polynomial block evaluates the required mathematical function to a first level of accuracy. This initial result is then used to initialise a CORDIC algorithm in an associated CORDIC block in order to refine the approximation of the mathematical function to the required level of accuracy. Such a two-step process is argued to reduce the storage requirements that might be required in order to evaluate a mathematical function to a desired level of accuracy, while also being faster than utilising a CORDIC algorithm alone.

The Claims

9 The application currently comprises two primary independent claims, as follows:

1. Apparatus configured to evaluate a predetermined mathematical function for a received input value, the apparatus comprising:

a memory configured to store values representing a predetermined set of polynomial functions which approximate the predetermined mathematical function over a respective set of domain intervals;

a polynomial hardware block implemented in fixed logic circuitry configured to:

identify a domain interval containing the received input value over which the predetermined mathematical function can be evaluated, the predetermined function over the identified interval being approximated by a polynomial function for which values are stored in the memory;

evaluate the polynomial function for the received input value using the stored values representing the polynomial function over the identified interval to calculate a first evaluation of the predetermined mathematical function for the received input value, the first evaluation having an accuracy less than a desired accuracy; and

generate as an intermediate output the first evaluation of the predetermined mathematical function; and

a CORDIC hardware block implemented in fixed logic circuitry for performing a CORDIC algorithm, the CORDIC hardware block being coupled to the polynomial hardware block and configured, in fixed logic circuitry, to:

receive the intermediate output of the first evaluation of the predetermined mathematical function for the received input value calculated by the polynomial block;

initialise the CORDIC algorithm using the first evaluation of the predetermined mathematical function;

implement the CORDIC algorithm to perform a plurality of iterative calculations to calculate a refined evaluation of the predetermined mathematical

function for the received input value, the refined evaluation having an accuracy of at least the desired accuracy; and

output the refined evaluation.

19. A computer-implemented method of evaluating a predetermined mathematical function for a received input value at an apparatus comprising a memory, a polynomial hardware block implemented in fixed logic circuitry and CORDIC hardware block implemented in fixed logic circuitry, the CORDIC hardware block being coupled to the polynomial hardware block, the method comprising:

at the polynomial hardware block:

identifying a domain interval containing the received input value over which the predetermined mathematical function can be evaluated, the predetermined mathematical function over the identified interval being approximated by a polynomial function;

evaluating a polynomial function for the received input value using values stored in the memory representing the polynomial function over the identified interval to calculate a first evaluation of the predetermined mathematical function for the received input value, the first evaluation having an accuracy less than a desired accuracy; and

generating an intermediate output for the first evaluation of the predetermined function;

at the CORDIC hardware block:

receiving the intermediate output of the first evaluation of the predetermined mathematical function for the received input value calculated by the polynomial block;

initialising a CORDIC algorithm using the first evaluation of the predetermined mathematical function;

implementing the CORDIC algorithm to perform a plurality of iterative calculations to calculate a refined evaluation of the predetermined mathematical function for the received input value, the refined evaluation having an accuracy of at least the desired accuracy; and

outputting the refined evaluation.

10 I would also note that there are a number of subsidiary independent claims, as follows:

38. A method of manufacturing, using an integrated circuit manufacturing system, an apparatus as claimed in any of claims 1 to 18, or 37.

39. An integrated circuit definition dataset that, when processed in an integrated circuit manufacturing system, configures the system to manufacture an apparatus as claimed in any of claims 1 to 18 or 37.

40. A non-transitory computer readable storage medium having stored thereon a computer readable description of an integrated circuit that, when processed in an integrated circuit manufacturing system, causes the integrated circuit manufacturing system to manufacture an apparatus as claimed in any of claims 1 to 18, or 37.

41. An integrated circuit manufacturing system configured to manufacture an apparatus as claimed in any of claims 1 to 18, or 37.

42. An integrated circuit manufacturing system comprising:

a non-transitory computer readable storage medium having stored thereon a computer readable integrated circuit description that describes an apparatus as claimed in any of claims 1 to 18, or 37;

a layout processing system configured to process the integrated circuit description so as to generate a circuit layout description of an integrated circuit embodying the apparatus; and

an integrated circuit generation system configured to manufacture the apparatus according to the circuit layout description.

43. An apparatus configured to perform the method of any of claims 19 to 36.

The Law

11 Section 1(2) of the Act states:

> *1(2) It is hereby declared that the following (amongst other things) are not inventions for the purpose of the Act, that is to say, anything which consists of-*
> *(a) A discovery, scientific theory or mathematical method;*
> *(b) A literary, a dramatic, musical or artistic work or any other aesthetic creation whatsoever;*
> *(c) A scheme, rule, or method for performing a mental act, playing a game or doing business, or a program for a computer;*
> *(d) The presentation of information;*
>
> *But the foregoing provisions shall prevent anything from being treated as an invention for the purposes of the Act only to the extent that a patent or application for a patent relates to that things as such.*

12 The provisions of Section 1(2) were considered by the Court of Appeal in *Aerotel Ltd v Telco Holdings Ltd and Macrossan's Application*[1] where a four step test was set out to decide whether a claimed invention was excluded from patent protection:

> *(1) Properly construe the claim;*
> *(2) Identify the actual contribution;*
> *(3) Ask whether it falls solely within the excluded subject matter;*
> *(4) Check whether the actual or alleged contribution is actually technical in nature.*

13 It was stated by Jacob LJ in *Aerotel* that the test is a re-formulation of and is consistent with the previous 'technical effect approach with rider' test established in previous UK case law. Kitchen LJ noted *in HTC v Apple*[2] that the *Aerotel* test is followed in order to address whether the invention makes a technical contribution to the art, with the rider that novel or inventive purely excluded matter does not count as a 'technical contribution'.

14 Lewison J in *AT&T/CVON*[3] set out five signposts that he considered to be helpful when considering whether a computer program makes a technical contribution. Lewison LJ reformulated the signposts in *HTC v Apple* in light of the decision in *Gemstar*[4]. The signposts are:

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[1] *Aerotel Ltd. V Telco Holdings and Macrossan's Application* [2006] EWCA Civ 1371
[2] *HTC Europe Co Ltd v Apple Inc* [2013] EWCA Civ 451
[3] *AT&T Knowledge Venture/CVON Innovations v Comptroller General of Patents* [2009] EWHC 343 (Pat)
[4] *Gemstar-TV Guide International v Virgin Media Ltd* [2010] RPC 10

i) Whether the claimed technical effect has a technical effect on a process which is carried on outside the computer.
ii) Whether the claimed technical effect operates at the level of the architecture of the computer; that is to say whether the effect is produced irrespective of the data being processed or the applications being run.
iii) Whether the claimed technical effect results in the computer being made to operate in a new way.
iv) Whether the program makes the computer a better computer in the sense of running more efficiently and effectively as a computer.
v) Whether the perceived problem is overcome by the claimed invention as opposed to merely being circumvented.

Analysis

15 I will use the *Aerotel* approach in my analysis to determine whether the invention relates to a program for a computer as such and/or a mathematical method as such.

(1) Properly construe the claim

16 During the rounds of amendment, the claims were amended to include the following features:

‘ a polynomial **hardware** block **implemented in fixed logic circuitry**’

‘ a CORDIC **hardware** block **implemented in fixed logic circuitry** for performing a CORDIC algorithm, **the CORDIC hardware block being coupled to the polynomial hardware block and configured, in fixed logic circuitry**’

17 The applicant has based much of their argument on the limitation of the claim to the hardware blocks being implemented in fixed logic circuitry. The invention as set out in the application as filed is described more generally and is concerned with a method which could be implemented either as a computer program or as some form of hardware. The application states that the invention might be put into practice through the use of any suitable hardware, software or combination thereof – see, for example, page 26, line 22 through to page 27, line 22. The only explicit reference to “fixed logic circuitry” in the description is found on page 26. It is mentioned as an example, within brackets, to describe what a notional hardware implementation of the invention may comprise.

18 During the hearing Mr Turner explained that the term ‘fixed logic circuitry’ refers to a series of hardware components such as gates, transistors, resistors, and the like which essentially embody the functionality of the claim itself. Furthermore, he explained that the claims were not intended to relate to a piece of general-purpose hardware which could be programmed to carry out the functionality of the claim. The claims are intended to relate to a very particular arrangement of hardware elements, albeit one claimed functionally. I can agree with this definition. Logic devices may be fixed or programmable. A fixed logic device is manufactured to perform a specific logic function at the time of manufacture, which cannot be altered thereafter. Furthermore, it would be readily apparent to the skilled reader, in relation to this application, that such a fixed logic circuit would comprise an arrangement of components such as gates, transistors and registers, the interconnections between

those components being fixed and unalterable. As such, I am happy to accept the interpretation of the term as it was put to me at the hearing.

19 Mr Turner referred me to the embodiment of part the invention illustrated in Figure 5 which is an example of a hardware implementation of the CORDIC hardware block:

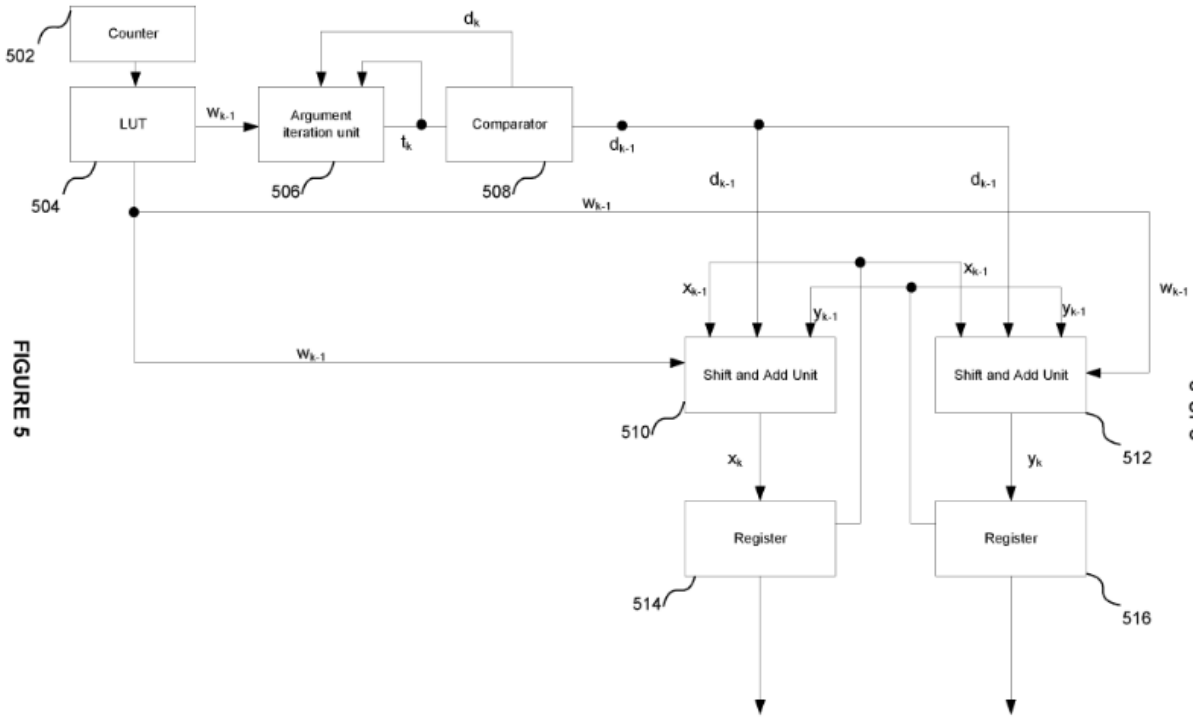

FIGURE 5

20 The operation of the circuit is described on pages 24 and 25 of the specification:

> "Figure 5 shows an exemplary hardware implementation of the implementing unit 216 for implementing the CORDIC algorithm described above in the form of a logic circuit.
>
> The implementing unit comprises a counter 502; LUT 504; an argument iteration unit 506; a comparator 508; two shift and add units 510 and 512; and two registers 514 and 516.
>
> The operation of the circuit is as follows. Counter 502 maintains a count of the iteration number *k* being performed by the CORDIC calculation unit. The value '*k*' is output to the LUT 504. The LUT stores the set of discrete bases w_k. The LUT outputs the constant w_{k-1} for iteration number *k* into the argument iteration unit 506. The unit 50 has also previously received as inputs d_{k-1} from comparator unit 508 and t_{k-1} output from the unit 506 in the previous iteration *k*-1 of the algorithm. The unit 506 operates to calculate the value t_k in accordance with equation (12). The output from unit 50 is fed into comparator 508. The value of t_k is also fed back to the argument iteration unit 506 for use in calculating the argument value t_{k+1} in the subsequent $(k+1)^{th}$ iteration.
>
> The comparator 508 compares the value of t_k with the thresholds in accordance with equation (13) in order to calculate the value d_k. The value of d_k is fed back to the argument iteration unit 506 for use in calculating the argument value t_{k+1} in the subsequent $(k+1)^{th}$ iteration. The values *d* (e.g. d_{k-1} in the k^{th} iteration) calculated by the comparator are input into the shift and add units 510 and 512.

> For the k'th iterative calculation, each of the shift and add units 510 and 512 receive as inputs: d_{k-1} calculated by the comparator unit; w_{k-1} output from the LUT 504; and x_{k-1} and y_{k-1} output from registers 514 and 516 respectively. Each of shift and add units 510 and 512 are configured to perform the iterative calculation specified in equation (19) and (20) respectively in dependence on their inputs. The output of the units 510 and 512 is fed into registers 514 and 516 respectively. Registers 514 and 516 therefore store the most recent evaluation of the trigonometric functions (i.e. the evaluation calculated from the current iterative calculation)."

21 The specification also includes a description of how the invention may be implemented as an integrated circuit and defined by an integrated circuit definition dataset which is processed at an integrated circuit manufacturing system. I note that, in relation to the polynomial block, the specification refers to one of the applicant's earlier PCT applications WO2005/116862. In this application it is clearly envisaged that the polynomial block could be implemented as a hardware circuit. It is apparent to me that a specific embodiment in fixed logic circuitry is envisaged in the specification, as is described for the CORDIC block in Figure 5 and the text quoted above.

22 Overall I construe the restriction of the claim to fixed logic circuitry as restricting the claim to specifically designed hardware blocks made up of circuit components which are fixed and are not programmable. Thus the polynomial hardware block and the CORDIC hardware block both relate to physical fixed circuitry which each relate only to one function, namely, to evaluating polynomial functions and to performing the CORDIC algorithm respectively. The claim does not cover implementations of the invention in software, firmware, field-programmable gate Arrays (FPGAs) or the like, albeit that the disclosed algorithms for evaluating the predetermined mathematical functions could be implemented in other ways. Nor does the claim cover implementations whereby program instructions are stored on a non-volatile memory such as a ROM. It is restricted to implementations in fixed circuitry.

23 I note that the applicant highlighted in their skeleton argument, and at the hearing, that there are particular benefits to implementing the invention using this hardware arrangement. In paragraph 18 of their skeleton it is stated:

> *"18. The evaluation of the function by the polynomial hardware block can therefore be an accuracy **less** than a desired accuracy since the evaluation result will be refined by the CORDIC hardware block. This enables the values representing the polynomial functions to be stored in the memory with a reduced precision, thus requiring a reduced memory footprint and saving on-chip real estate."*

24 According to the applicant's skeleton the inventors have found an overall benefit that flows from the claimed dual approach that permits an evaluation result to be generated that has the desired accuracy faster than a pure CORDIC approach whilst advantageously reducing memory requirements compared to a pure polynomial approach. These comments are also reflected on page 10 of the specification. Mr Turner emphasised that the desired accuracy is maintained in the claimed apparatus. These advantages are particularly important when implemented in hardware in the processing cores designed by the applicant where on-chip real estate is at a premium and processing latency can be very important.

25 I am prepared to accept that these advantages do arise out of the claimed invention, implemented in fixed logic circuitry.

26 The claim is therefore directed towards a hardware device that comprises a memory and a polynomial hardware block implemented in fixed logic circuitry that is connected to a CORDIC hardware block implemented in fixed logic circuitry. The arrangement is such that a predetermined mathematical function can be determined for a received input value through running an initial calculation in the polynomial block to determine an intermediate output which is subsequently passed to the CORDIC block that runs a subsequent calculation to output a refined, more accurate value.

(2) Identify the contribution

27 Identifying the contribution in the second step of this test is critical and I refer to the following paragraph in *Aerotel* for guidance:

> *"43. The second step – identifying the contribution – is said to be more problematical. How do you assess the contribution? Mr Birss submits the test is workable – it is an exercise in judgement probably involving the problem said to be solved, how the invention works, what its advantages are. What has the inventor really added to human knowledge perhaps best sums up the exercise. The formulation involves looking at the substance not form – which is surely what the legislator intended."*

28 As the application has not yet been searched, I can only determine what I believe to be the alleged contribution.

29 I have construed the limitation of the claim to "fixed logic circuitry" above. The applicant has identified specific advantages to the invention when implemented in fixed logic circuitry, as I have detailed above. These are a reduction in the silicon area required for the fixed logic circuitry which arises out of the ability to use fewer values by the polynomial hardware block compared with using a polynomial hardware block alone, and also an increase in processing speed when compared with using a pure CORDIC hardware block. These sorts of advantages are commonly claimed in inventions where the computer program exclusion is at issue, it often being argued that, in a generic sense, computers run faster or require fewer resources when running a particular computer program as compared to certain prior art computer programs. I would however comment that, in the present case where the invention is implemented as fixed logic circuitry, I can see that these can be very real benefits, particularly in systems where silicon space and processing and memory capacity may be constrained such as, for example in processing cores for small Internet of Things (IoT) devices. These advantages do therefore, in my view, form part of the contribution.

30 I believe that the contribution of the claimed invention is:

> An apparatus for evaluating a predetermined mathematical function for a received input that comprises a polynomial hardware block implemented in fixed logic circuitry that performs an initial calculation to determine an initial evaluation of the predetermined mathematical function, coupled to a CORDIC hardware block implemented in fixed logic circuitry that receives the initial evaluation from the polynomial block and performs a second calculation to

refine the evaluation to a greater level of accuracy, the apparatus resulting in a reduced storage requirement and a reduction in processing latency when compared with using either the polynomial hardware block or the CORDIC hardware block alone.

31 This is consistent with the contribution identified by Mr Turner in his skeleton and at the hearing.

(3) and (4) Ask whether the contribution falls solely within the excluded subject matter; and check it is actually technical in nature

32 For convenience I will consider steps (3) and (4) together.

33 The applicant's main argument is that, as the invention is implemented as fixed logic circuitry, the claimed invention now relates purely to a new arrangement of hardware and there is simply no computer program or 'set of instructions' present in the contribution at all, and nor do the claims cover a set of instructions stored or otherwise available on any medium. Rather, it is the fixed logic circuitry itself which implements the claimed invention and provides the claimed functionality. The invention cannot therefore be said to lie in the excluded field of a program for a computer as there is simply no computer program

34 Mr Turner argued that the present invention is distinguished from that in *Gale's Application*[5] and referred me to another recent Office decision, BL O/420/21[6], in support of his arguments. In this decision the hearing officer considered another application by Imagination Technologies directed towards a similar technology. While in the application being considered in that hearing reference was made to 'fixed function circuitry', rather than 'fixed logic circuitry', it was argued that the terms effectively related to the same thing – an arrangement of gates, transistors, registers and the like that act to achieve a very specific function. It was argued that, importantly, with both applications the terms implied that there is no processor which needs to be told what to do with any stored instructions.

35 Merely embodying an invention in hardware does not necessarily avoid the computer program exclusion. In *Gale* the invention (calculating a square root) was embodied as a series of computer instructions stored on a read-only memory (ROM) which were then read by a processor and enacted on a general-purpose computer to perform certain mathematical operations. The Court of Appeal rejected the notion that an otherwise excluded computer program could become patentable if the program instructions were embodied on a ROM. On page 326 line 48 to page 327 line 3 Nichols LJ stated:

> *"I approach the substantial issue in this case, therefore, on the footing that it is convenient and right to strip away, as a confusing irrelevance, the fact that the claim is for "hardware". The claim in the specification is, in substance, a claim to a series of instructions which incorporate Mr. Gale's improved method of calculating square roots. It is a claim to electronic circuitry in the form of a ROM which is only distinguishable from other electronic circuitry in the form of a ROM by the sequence*

[5] *Gale's Application* [1991] RPC 305
[6] Imagination Technologies Limited BL O/420/21

of instructions it contains. As such those instructions are not patentable, because they constitute a computer program."

36 Nichols LJ did go on to consider whether there was a technical effect either inside or outside the computer but concluded that there was not.

37 Mr Turner also referred to *Fujitsu*[7], which related to a similar situation where there were a series of instructions stored on a ROM. It is clear from these cases that the substance of the claim must be considered and that the mere mention of hardware in the claim, such as in *Gale* or *Fujitsu*, is not enough to avoid the computer program exclusion. On page 326 lines 6-22 Nichols LJ referred to the EPO Technical Board of Appeal decision T22/85 IBM Corp./Document abstracting and retrieving[8] as follows (emphasis mine):

> *"This accords with the approach adopted by the European Patent Office. In IBM Corp./Document abstracting and retrieving (Decision T22/85), [1990] E.P.O.R. 98, the Technical Board of Appeal rejected an application for a patent related to a method for automatically abstracting and storing documents in an information storage and retrieval system and to a corresponding method for retrieving a document from the system. The board held that any new concept in the application could he only in the prescribed procedures, and those procedures or rules had no technical character but were of a purely intellectual nature. In paragraph 14, the board added:*
>
> > *"The foregoing considerations have been made mainly on the basis that the claimed systems and methods would involve a conventional computer controlled by a software program... Analogous considerations, however, apply in the case where the control of the computer would be effected by hardware (specifically designed logical means), an option also falling within the scope of the claims, as the choice between the two possibilities is not of an essential nature but is based on technical and economical considerations which bear no relationship to the inventive concept as such.""*

38 The reference to this EPO case in *Gale* strengthens the argument that merely implementing an invention in hardware, even if the hardware in question is specifically designed logical means, is not enough to avoid the computer program exclusion if the choice between the two possibilities (implementation in hardware and implementation in software) is not of an essential nature. I do however note that the EPO case relates to the control of a conventional computer by a software program. The present invention does not directly relate to a hardware implementation of such an arrangement as it does not directly control a conventional computer except to the extent that it potentially receives an input from such a computer and sends an output to the computer in question. I think that the key distinction here is that, in the claimed invention, there is no 'control of the computer' in the sense intended in this EPO case. The claimed invention is effectively a component which operates to provide predetermined mathematical functions when requested to do so by a processor or similar. The claimed invention does not act in any way to deliver instructions or otherwise direct how the computer operates. It merely provides an output when provided with a suitable input, with the utility or purpose of that output being decided

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[7] *Fujitsu Ltd's Patent Application* [1997] RPC 608

[8] T22/85 IBM Corp./Document abstracting and retrieving [1990] E.P.O.R. 98

elsewhere within the computer. The relevance of this EPO case therefore stands or falls with the relevance of *Gale* itself.

39 Mr Turner submitted that the present case is distinguished from *Gale* because, rather than relating to instructions stored on circuitry, the invention is implemented as circuitry itself. There are no instructions at all.

40 I need to carefully consider the relevance of the teaching in *Gale* to the present case. Just as in *Gale*, the algorithm used to evaluate mathematical functions can, according to the specification, be implemented in either software or hardware. The claim limits the invention to implementation as fixed logic circuitry which I have construed above. This is not the same as the limitation in *Gale*, which was to instructions stored on a ROM. The question I need to answer is, in the present case, is the hardware a “confusing irrelevance” which should be stripped away, or does it form part of the substance of the invention?

41 Having considered this carefully, and having come to the conclusion that the embodiment of the invention as fixed logic circuitry has real benefits in terms of silicon area and processing time and these therefore form part of the contribution, on the balance of probabilities I conclude that the fixed logic circuitry is part of the substance of the invention, particularly given that a consequence of this implementation is that there are no program instructions stored in the system for carrying out the polynomial and CORDIC calculations. I therefore conclude that, in the present case, the limitation is not a confusing irrelevance but a substantial part of the invention. The present case is therefore distinguished from *Gale*.

42 Further considering the contribution, I note that it relates to fixed logic circuitry designed to evaluate a predetermined mathematical function in the form of a polynomial hardware block and a CORDIC hardware block. The combination of the two blocks of fixed logic circuitry results in an apparatus in which less memory is needed to store the values which represent the polynomial function compared to using the polynomial block alone, thereby requiring a smaller silicon footprint, and which has less latency (and so requires less processing resource) than an apparatus which uses the CORDIC block alone. This results in a better tool for calculating mathematical functions, embedded as fixed logic circuitry into a system, which is available for any program to make use of. Thus the technical effect is at the architecture level of the computer. Moreover a computer incorporating this circuitry will be a better computer in that it will run more efficiently and effectively as a computer whenever any program makes use of this circuitry to evaluate mathematical functions.

43 Given my analysis above I do not need to consider the *AT&T* signposts in detail. I however note that my analysis above is consistent with signposts ii) and iv). The claimed technical effect operates at the level of the architecture of the computer and the effect is produced irrespective of the data being processed or the applications being run in accordance with signpost ii). The invention also could be said to result in a better computer in the sense of running more efficiently and effectively as a computer, in accordance with signpost iv). I therefore conclude that the identified contribution does involve a technical contribution.

44 On balance I find the arguments that have been presented to me on this issue persuasive. I think it is worth highlighting that I do not believe that merely adding a term such as ‘fixed logic circuit’ into any claim will necessarily enable the computer exclusion to be avoided. Rather, every case must be considered on its merits. However, I am happy that, having construed the claim as I have, the claimed invention in the current application can be considered to relate in substance to a hardware arrangement. The claims are effectively directed towards a subset of the possible embodiments of the wider concept disclosed in the application, rather than an attempt to circumvent the computer program exclusion by dressing up a computer program in hardware terms. I therefore conclude that the claimed invention does not lie solely in the excluded field of a program for a computer as such.

45 I will also consider the claimed invention in relation to the mathematical method exclusion. In *Gale* Nichols LJ held on page 327 that the application of the mathematical formulae for the purpose of writing computer instructions was sufficient to dispose of the contention that a claim was directed towards a mathematical method as such – he was not claiming a mathematical method but rather a computer program which ran the mathematical method. Similarly in the present case I do not consider the contribution to fall solely in the excluded field of a mathematical method as such. Rather it relates to a hardware arrangement which enables the mathematical processing to take place.

46 I note that my conclusion is consistent with that of the hearing officer in BL O/420/21.

Conclusion

47 I have found that the claimed invention is not excluded from patentability under section 1(2)(a) or section 1(2)(c).

48 The application has yet to be searched and there remains a need to consider the wider patentability of the claims. I therefore refer the application back to the examiner for further examination.

Appeal

49 Any appeal must be lodged within 28 days after the date of this decision.

B Micklewright

Deputy Director, acting for the Comptroller